# Steffi Roy

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## Education

**University of Florida** ***2021 — 2023***
MS in Electrical and Computer Engineering GPA: 3.6/4
**Mahindra Ecole Centrale, Hyderabad** ***2016 — 2020***
Bachelor of Technology in Electrical and Electronics CGPA: 9.3/10

### *Relevant Coursework*

Automated Hardware/Software Verification, Advance Hardware Security, Machine Learning, Cad for Hardware Security Validation, Computer Architecture, Reconfig Computing, Machine Learning, Quantum Computing, Data Structures, Digital Signal Processing, VLSI Circuits, Computer Network.

## Research Experience

**University of Florida, Research Assistant** *Dec 2022 – Jan 2021*

- Conducted research in the FICS Lab on hardware security, developing methodologies for secure electronic design automation (EDA), side-channel resilience for neural networks, and hardware metering protocols.
- Proposed novel paradigms for semiconductor IP protection using secure and private function evaluation (SFE-PFE), advancing privacy-preserving security protocols.

## Professional Experience

**Texas Instruments, Design Verification Engineer** *Present – Aug 2023*

- SoC-level verification for IPs, including Flash Subsystem, XSPI, Hyperbus, Phase-Locked Loop (PLL) and Real-Time Clock (RTC), by developing detailed test plans, coding tests and performing debugging.
- Automated processes and improved verification workflows by developing various scripts and tools to save time in debugging and verification.

**Microsoft, Sillicon Engineer Intern** *Apr 2023 – Jan 2023*

- Planned and created a full chip test between SoC and Southbridge AXI Interconnect.
- Created the coverage, SVA build, ran regressions, and assisted in UVM error debugging for Xbox.

**Gallium Arsenide Enabling Technology, Chip Testing Intern** *July 2019 – May 2019*

- Learned about design, fabrication, assembly, and testing processes/techniques involved in the manufacturing of GaAs wafers for satellites by working with scientists and engineers. Operated qualification checks.

**Defense Research Development Laboratory, Autopilot Design Intern** *July 2018 – April 2018*

- Simulated linear control Autopilot design for a 3-DOF model of a tactical guided missile using MATLAB. Designed compensators, PID controller, and band-pass filter.
- Achieved optimal performance for phase margins, gain margins, and rise time with low noise.

## Research Projects

**Privacy-Preserving Electronic Design Automation** *(University of Florida)*

- Defined the Garbled EDA framework, highlighting its use of multiparty computation to safeguard IP, CAD tools, and PDKs, and developed implementation methodologies addressing both resource utilization and security against malicious adversaries.
- Authored introducing the problem, outlining adversary models, and detailing the secure function evaluation (SFE) and private function evaluation (PFE) protocols for EDA tool security.

**Active IC Metering Protocol Security** *(University of Florida)*

- Designed and implemented secure IC metering protocols using Bellare-Micali and Naor-Pinkas oblivious transfer (OT) techniques, enhancing privacy and protection against malicious adversaries in bus-scrambling IC activation schemes.
- Analyzed security vulnerabilities in existing protocols, proposed countermeasures for attacks like fault injection and MITM, and demonstrated improved protocol efficiency under Diffie-Hellman assumptions.

**Hardware-Garbled Neural Networks (HWGN2): Secure DL Inference** *(University of Florida)*

- Conducted an extensive review of existing methods in side-channel attacks, garbled circuits, and secure deep learning accelerators, summarizing findings to provide a comparative evaluation.
- Analyzed experimental results to highlight HWGN2's advancements, including improved resilience to side-channel attacks and efficient secure inference on FPGA platforms and its advantages over existing solutions.

**HPA Linearization for Next-Generation Broadcasting Systems** *(Mahindra Ecole Centrale)*

- Assisted in implementing algorithms in MATLAB for "HPA Linearization for Next Generation Broadcasting Systems With Fast Convergence-Digital Predistortion" (IEEE Transactions on Broadcasting, 2021).
- Developed MATLAB code to analyze/plot the performance of digital predistortion (DPD) techniques on high power amplifiers (HPA) for digital terrestrial television (DTT) broadcasting systems, optimizing for rapid convergence.

**Constant Modulus Algorithm (CMA) for Adaptive Beamforming** (*Defence Research Development Lab)*
- Investigated the Constant Modulus Algorithm (CMA) for adaptive beamforming, implementing it in python and Verilog for software-defined radios (SDR) to achieve phase alignment across antenna arrays.
- Analyzed convergence behavior and amplitude response, exploring CMA's potential for adaptive beamforming in real-time missile applications, challenges such as multipath environments and hardware integration.

## Presentations

- **Active IC Metering Protocol Security with Oblivious Transfer** SRC TECHCON 2022, presented the security protocols for active IC metering and oblivious transfer applications.
- **HWGN2: Side-Channel Protected Neural Networks** SPACE Conference 2022, presented research on side-channel resilient neural networks using secure and private function evaluation.
- **Maestro XML Diff tool** DVCON 2025, present demo of the tool utilizes libraries in python to help DV Engineer to keep track of with Maestro xml updates.

## Technical Skills

**Programming:** Python, System Verilog/Verilog, C++, Assembly, Tcl, SQL

**Tools:** JasperGold, Gem 5, Pspice, Vivado, Virtuoso, Unix/Linux, MATLAB, Simvision, Git, ModelSim, LaTeX

## Publications

- M. Hashemi, **S. Roy**, F. Ganji, D. Forte, "Garbled EDA: Privacy-Preserving Electronic Design Automation," ICCAD, 2022.
- **S. Roy**, M. Hashemi, F. Ganji, D. Forte, "Active IC Metering Protocol Security with Oblivious Transfer," SRC TECHCON, 2022.
- M. Hashemi, **S. Roy** D. Forte, F. Ganji, "HWGN2: Side-Channel Protected Neural Networks," SPACE Conference, 2022.

## Achievements

**Scolarships**
- Merit Scholarship 100,000 INR awarded annually for academic performance in Undergrad.
- Awarded scholarship of 200,000 INR for performance in high school entrance examination.
- Awarded 5000 INR from CBSE School board for NCSC project.

**Hackathon**
- Chatbot Development: Placed **3rd** in a college, created a Zulip API-based chatbot for live news and weather updates using Python.
- TI DV Hackathon: Worked on a DV project based on Maestro xml diff tool to be showcased at **DVCON25**.
- Mozilla Hackathon: Developed a web extension using JavaScript, CSS, and HTML to censor profanity and replace words with emojis.

## Volunteer/Leadership Experience

- Mentored undergrad students on research and career development through the UF WECE and Gator Alumni networks.
- Organized events for the TI Robotics Club
- Conducted interactive science and math classes for children as part of the OUTREACH Club during undergrad.